MC74HC174A

Hex D Flip-Flop with Common Clock and Reset

High−Performance Silicon−Gate CMOS

The MC74HC174A is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D flip−flops with common Clock and Reset inputs. Each flip−flop is loaded with a low−to−high transition of the Clock input. Reset is asynchronous and active−low.

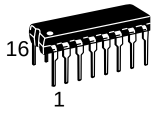
Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates
- Pb−Free Packages are Available*

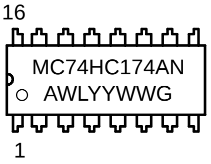
ON Semiconductor®

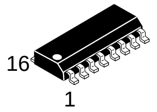
http://onsemi.com

MARKING DIAGRAMS

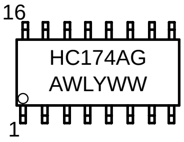


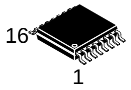
PDIP−16
N SUFFIX
CASE 648



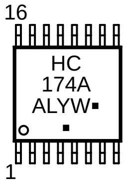


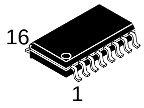
SOIC−16
D SUFFIX
CASE 751B



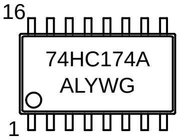


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G = Pb−Free Package
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

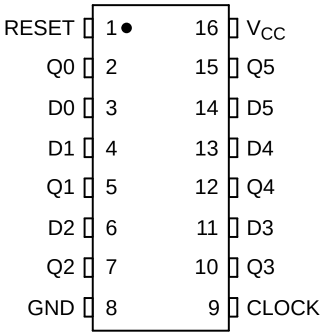


Figure 1. Pin Assignment

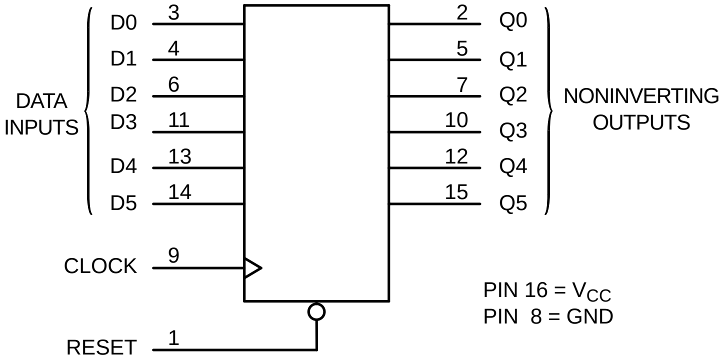


Figure 2. Logic Diagram

FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No Change
H	↓	X	No Change

DESIGN/VALUE TABLE

Design Criteria	Value	Units
Internal Gate Count*	40.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two−input NAND gate.

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC174AN	PDIP−16	500 Units / Rail
MC74HC174ANG	PDIP−16 (Pb−Free)	500 Units / Rail
MC74HC174AD	SOIC−16	48 Units / Rail
MC74HC174ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HC174ADR2	SOIC−16	2500 Units / Reel
MC74HC174ADR2G	SOIC−16 (Pb−Free)	2500 Units / Reel
MC74HC174ADTR2	TSSOP−16*	2500 Units / Reel
MC74HC174ADTR2G	TSSOP−16*	2500 Units / Reel
MC74HC174AFEL	SOEIAJ−16	2000 Units / Reel
MC74HC174AFELG	SOEIAJ−16 (Pb−Free)	2000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	− 0.5 to + 7.0	V
V_{IN}	DC Input Voltage	(Referenced to GND)	− 1.5 to V_{CC} + 1.5	V
V_{OUT}	DC Output Voltage	(Referenced to GND) (Note 1)	− 0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		± 20	mA
I_{OUT}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 50	mA
T_{STG}	Storage Temperature Range		− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	PDIP, SOIC, TSSOP	260	°C
T_J	Junction Temperature Under Bias		+ 150	°C
θ_{JA}	Thermal Resistance	PDIP SOIC TSSOP	78 112 148	°C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in.	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 100 > 500	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 5)	± 300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.
6. For high frequency or heavy load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage	(Referenced to GND) (Note 7)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types		− 55	+ 125	°C
t_r, t_f	CLOCK Input Rise and Fall Time (Figure 4)	V_{CC} = 2.0 V V_{CC} = 3.3 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 700 500 400	ns

7. Unused inputs may not be left open. All inputs must be tied to a high− or low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit −55°C to 25°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{OUT}\rvert \leq$ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{OUT}\rvert \leq$ 20 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq$ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq$ 4.0 mA $\lvert I_{OUT}\rvert \leq$ 5.2 mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq$ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq$ 4.0 mA $\lvert I_{OUT}\rvert \leq$ 5.2 mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0	4.0	40	160	μA

8. Information on typical parametric values, along with high frequency or heavy load considerations, can be found in the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55°C to 25°C	≤85°C	≤125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 4 and 7)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 5 and 7)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 7)	2.0 4.5 6.0	110 21 19	140 28 24	160 32 27	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 4 and 7)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance, per Enabled Output (Note 10)	62	pF

10. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

				Guaranteed Limit						
			V_{CC}	−55°C to 25°C		≤85°C		≤125°C		
Symbol	**Parameter**	**Figure**	**V**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{su}	Minimum Setup Time, Data to Clock	6	2.0	50		65		75		ns
			4.5	10		13		15		
			6.0	9.0		11		13		
t_h	Minimum Hold Time, Clock to Data	6	2.0	5.0		5.0		5.0		ns
			4.5	5.0		5.0		5.0		
			6.0	5.0		5.0		5.0		
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock	5	2.0	5.0		5.0		5.0		ns
			4.5	5.0		5.0		5.0		
			6.0	5.0		5.0		5.0		
t_w	Minimum Pulse Width, Clock	4	2.0	75		95		110		ns
			4.5	15		19		22		
			6.0	13		16		19		
t_w	Minimum Pulse Width, Reset	5	2.0	75		95		110		ns
			4.5	15		19		22		
			6.0	13		16		19		
t_r, t_f	Maximum Input Rise and Fall Times	4	2.0		1000		1000		1000	ns
			4.5		500		500		500	
			6.0		400		400		400	

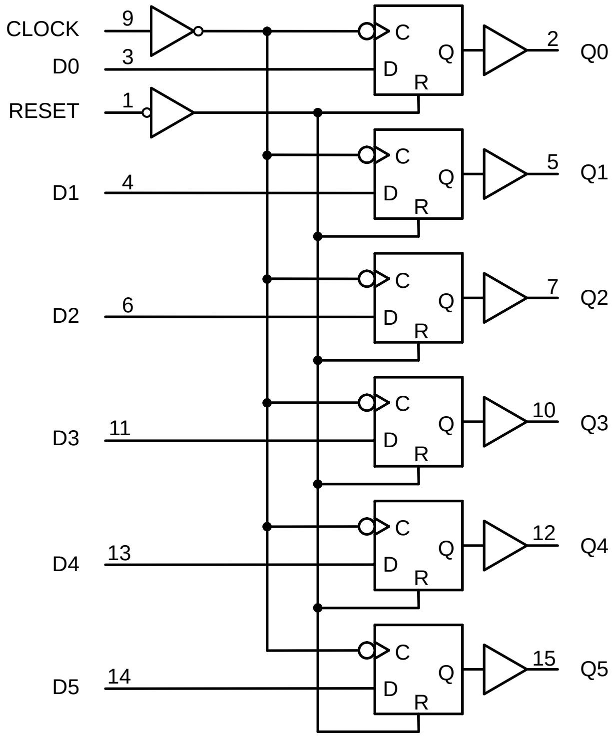


Figure 3. Expanded Logic Diagram

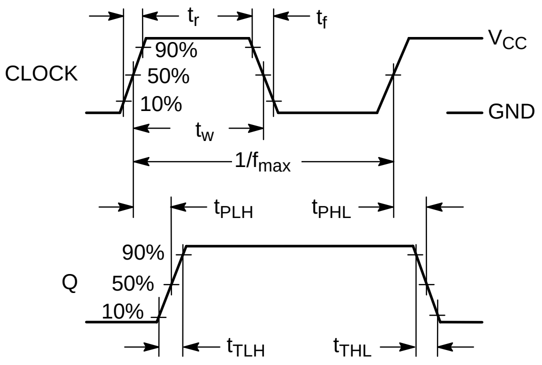


Figure 4. Switching Waveform

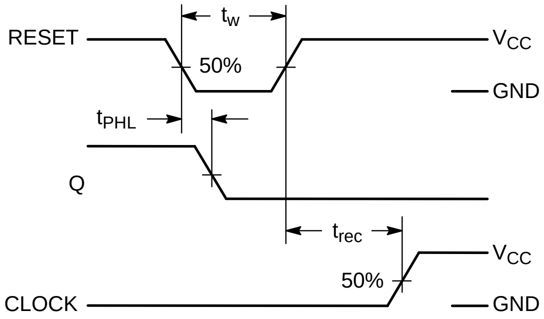


Figure 5. Switching Waveform

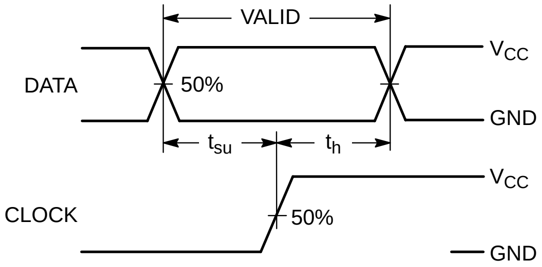
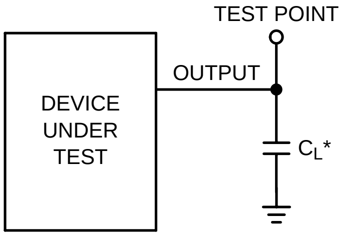


Figure 6. Switching Waveform

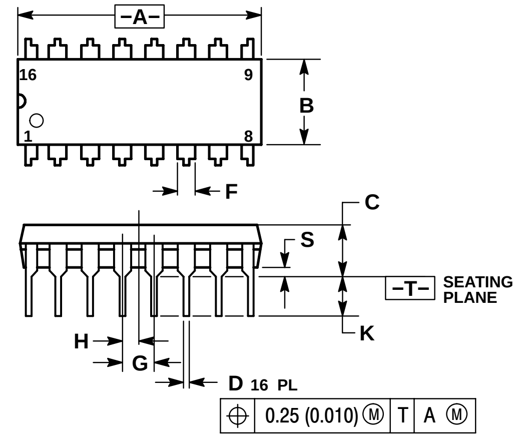


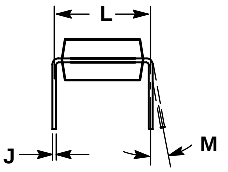
*Includes all probe and jig capacitance

Figure 7. Test Circuit

PACKAGE DIMENSIONS

PDIP−16
N SUFFIX
CASE 648−08
ISSUE T

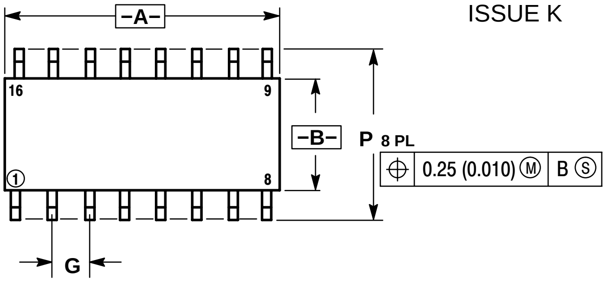


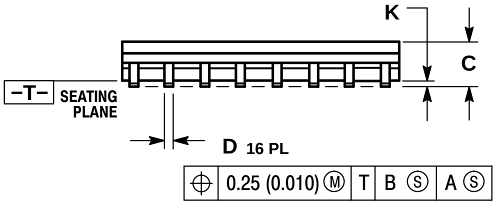


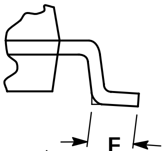
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

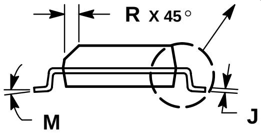
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE K





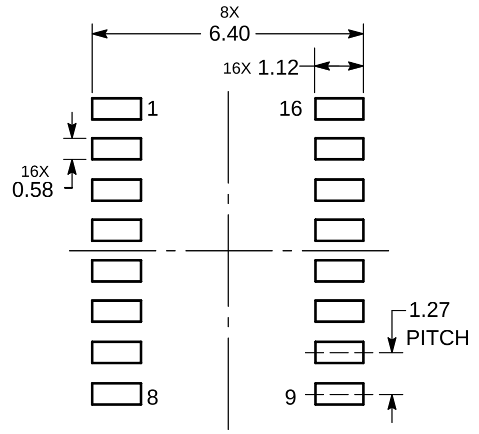




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

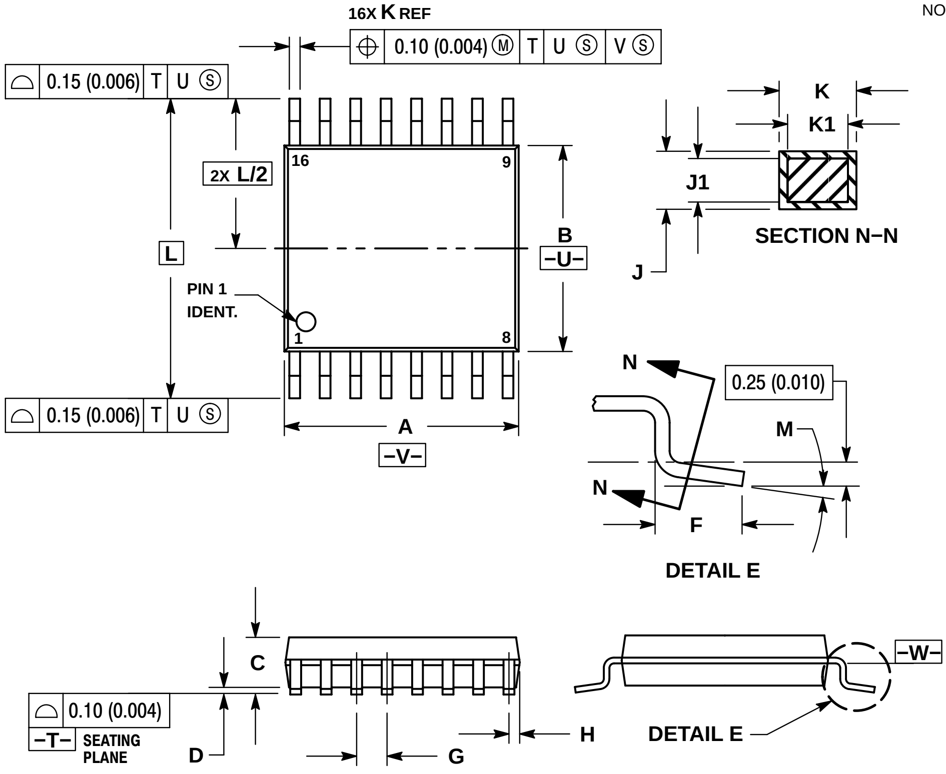
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

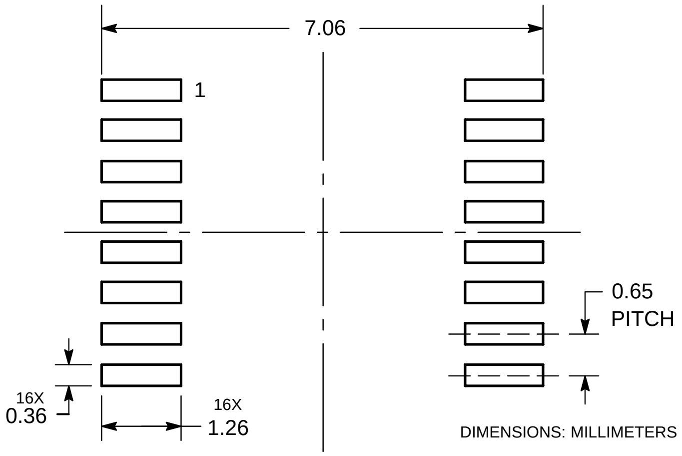
TSSOP−16
DT SUFFIX
CASE 948F−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

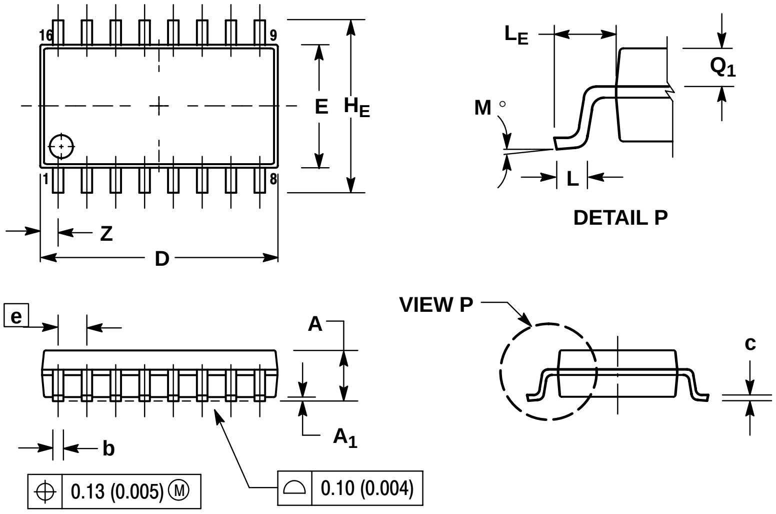
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

SOEIAJ−16
F SUFFIX
CASE 966−01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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